AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors which are disposed in said substrate and which include gate insulating films; and

an MOS type varactor element which is disposed in said substrate and which includes a gate insulating film, the thickness thereof being thinner than the thinnest gate insulating film among said gate insulating films of said MOS transistors, said varactor element including a second conductivity type well in said first conductivity type substrate, two second conductivity type diffusion regions in a surface of said second conductivity type well, said two diffusion regions having higher impurity concentrations than said well and being directly connected to a same well terminal, said gate insulating film of said varactor element being on said surface between said two diffusion regions, and a gate electrode on said gate insulating film between said two diffusion regions.

2. (original) A semiconductor integrated circuit device according to Claim 1, wherein a maximum gate voltage applied to

said MOS type varactor element is lower than a maximum gate voltage applied to said MOS transistors.

3. (original) A semiconductor integrated circuit device according to Claim 1, wherein said substrate is a semiconductor substrate.

4. (original) A semiconductor integrated circuit device according to Claim 2, wherein said substrate is a semiconductor substrate.

5. (currently amended) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

plural MOS transistors which are disposed in said substrate and which include gate insulating films, said MOS transistors not being part of a varactor; and

an MOS type varactor in said substrate and spaced from said plural MOS transistors and which includes a gate insulating film, a thickness of said gate insulating film of said varactor being thinner than the thinnest gate insulating film among said gate insulating films of said plural MOS transistors, said varactor including a second conductivity type well in an upper surface of said first conductivity type substrate, two first conductivity type diffusion regions in an upper surface of said second conductivity type well, said two diffusion regions having higher impurity concentrations than said well and being directly connected to a same ground terminal, said gate insulating film of

said varactor being on said upper surface of said well between said two diffusion regions, and a gate electrode on said gate insulating film between said two diffusion regions.

6. (previously presented) The device of claim 5, wherein said gate insulating film of said varactor and said gate insulating films of said plural MOS transistors are at a same level of the device.

7. (previously presented) The device of claim 5, wherein the thickness of said gate insulating film of said varactor is about three quarters of a thickness of said gate insulating films of said plural MOS transistors.

8. (previously presented) The device of claim 7, wherein the thickness of said gate insulating film of said varactor is about 6 nm and the thickness of said gate insulating films of said plural MOS transistors is about 8 nm.

9. (previously presented) The device of claim 5, wherein said plural MOS transistors include an N-channel MOS transistor and a P-channel MOS transistor.

10. (previously presented) The device of claim 1, wherein said gate insulating film of said varactor element and said gate insulating films of said MOS transistors are at a same level of the device.

11. (previously presented) The device of claim 1, wherein the thickness of said gate insulating film of said

varactor element is about three quarters of a thickness of said gate insulating films of said MOS transistors.

12. (previously presented) The device of claim 11, wherein the thickness of said gate insulating film of said varactor element is about 6 nm and the thickness of said gate insulating films of said MOS transistors is about 8 nm.

13. (previously presented) The device of claim 1, wherein said MOS transistors are spaced from said varactor element and include an N-channel MOS transistor and a P-channel MOS transistor.

14. (currently amended) The device of claim 9, wherein the first conductivity type ~~said substrate~~ is a P type and the second conductivity type is N type, ~~and said MOS type varactor has an N well disposed in an upper surface of the P type substrate, a gate insulating film disposed on the N well, a gate electrode disposed on the gate insulating film, P^+ diffusion regions placed in two areas in a surface of the N well sandwiching the gate electrode,~~ and further comprising an N^+ diffusion region placed in an area separated from directly under the gate electrode and the P^+ diffusion regions in the surface of the N well, and a P^+ diffusion region placed at a part of an area where the N well is not disposed in the upper surface of the P type substrate.